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(54) N-CHANNEL FIELD EFFECT TRANSISTOR

(71) We, NORTH AMERICAN ROCKWELL CORPORATION, a Corporation organized and existing under the laws of the State of Delaware, United States of America, having its principal place of business at 2300 East Imperial Highway, City of El Segundo, State of California, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an N-channel field effect transistor.

In present day microelectronics, increasing emphasis is being placed on the use of field effect transistors (FET's) since such transistors readily lend themselves to fabrication in high density integrated circuits. In enhancement mode FET's, source to drain conduction is dependent upon a channel which is electrostatically induced by a gate potential. An N-channel field effect transistor utilizes N-type conductivity material for the source and drain, and conduction therebetween occurs primarily by majority type free electrons. In a P-channel FET, source to drain current primarily is by majority hole carriers.

In most prior art silicon N-channel FET's, the insulation separating the channel from the gate electrode comprised SiO_2. In such a transistor, whether the oxide was grown thermally in an O_2 or H_2O atmosphere, an interfacial change occurred at the interface between the silicon channel and the silicon dioxide gate insulation. While the mechanism causing this interfacial change has not been explained, it manifests itself as an accumulation of positive charge within the SiO_2 or at the SiO_2/Si interface.

In a P-channel FET, the positive charge at the channel-gate insulation interface is not detrimental. Since, in a P-channel device conduction is by holes, the positive surface state prevents current from flowing between source and drain prior to application of a negative gate voltage. Moreover, this negative gate voltage must be increased to a value which will compensate for the interfacial positive charge before source to drain hole current is initiated.

A more serious problem arises because of interfacial charge in an N-channel field effect transistor. In such an N-channel transistor, the source and drain comprise regions of heavy donor concentration, and conduction is by electrons. Because of the positive interfacial charge at the channel/gate insulation interface, some current I_{DS} will flow between source and drain even when no external gate voltage is applied. Of course, I_{DS} will increase as a positive voltage is applied to the gate electrode. However, this current flow with zero applied gate voltage limits the usefulness of prior art N-channel FET's, particularly for digitial applications where it is desirable to have no output (i.e., zero current flow) until a non-zero gate voltage is applied.

To overcome this normally ON condition, prior art N-channel FET's typically were fabricated on a semicondutor substrate having a very high P-type dopant concentration. If a sufficiently high acceptor concentration were provided, the bulk charge density in the channel was sufficient to compensate for the positive interfacial charge. Thus, while this provided an FET which was OFF prior to application of a positive gate voltage, the high acceptor density degraded other transistor characteristics. In particular, such prior art N-channel FET's exhibited low values of breakdown voltage $V_{(BR)DSS}$ and high values of drain capacitance, which high capacitance reduced the maximum frequency of operation of the device. Moreover, these limitations inherent in prior art N-channel FET's made it diffi-

cult to produce complementary N- and P-channel devices having like characteristics of breakdown voltage, drain capacitance and speed.

These and other limitations of prior art N-channel enhancement mode field effect transistors are overcome in the FET according to the present invention, which provides a field effect transistor including a channel, an N-type source and drain, and a P-type isolation region completely separating the source from the channel over the whole area of the source-channel junction so that, over the said area, current cannot flow between the source and channel other than through the isolation region. This FET has essentially no source to drain current flow in the absence of an applied gate voltage, and has a higher breakdown voltage and lower drain capacitance than exhibited by N-channel enhancement mode transistors of the prior art. Consequently, the field effect device is useful in digital applications, and has potentially higher frequency capability than prior art N-channel FET's.

In performing the present invention there can be provided an N-channel enhancement mode field effect transistor comprising a semiconductor body having a low acceptor concentration. Diffused in the body are N-type source and drain regions, which regions define a channel therebetween. A P+ region of high acceptor concentration isolates the source from the channel; the P+ region extends the entire width of the channel, but only a fraction of the channel length.

In a first embodiment, the inventive field effect transistor is fabricated in bulk semiconductor, with the P+ isolation region completely surrounding the bottom and sides of the source. In a second embodiment, the FET is fabricated on a semiconductor film disposed on top of an electrically insulating substrate. The source, drain, channel, and P-type isolation regions each extend through the entire thickness of the semiconductor film, the isolation region being a fraction of the length of the channel and separating the N-type source from the channel.

In yet another embodiment of the present invention, the P+ region itself is provided with an electrical contact facilitating a four-terminal transistor, operable in both the enhancement and depletion modes, and having improved transconductance.

The field effect transistor may be fabricated by two subsequent diffusions through the source opening in the conventional FET mask. The first diffusion is of an acceptor type impurity, thereby forming the P+ region which eventually will isolate the source. Subsequently, a donor type impurity is diffused, through the same mask opening, thereby forming the source.

The invention will be described in more detail, by way of example, with reference to the accompanying drawings, in which:—

FIGURE 1 is a greatly enlarged, fragmentary sectional view of an N-channel field effect transistor in accordance with the present invention. In the embodiment illustrated, the transistor is fabricated in bulk semiconductor material.

FIGURE 2 is a graph showing the threshold and breakdown voltage characteristics of a typical N-channel FET fabricated in accordance with the present invention and having the configuration of FIGURE 1.

FIGURE 3 is a graph illustrating the drain current characteristics of a typical FET having the configuration of FIGURE 1. Illustrated are a family of I_{DS} versus V_{DS} curves for various values of V_{GS}.

FIGURE 4 is a graph illustrating the difference in threshold voltage between two N-channel FET's of like channel size, one in accordance with the prior art, the other in accordance with the present invention.

FIGURE 5 is a greatly enlarged, fragmentary sectional view of another embodiment of the inventive N-channel enhancement mode FET, as fabricated on a semiconductor thin film disposed atop an electrically insulating substrate.

FIGURE 6 shows a family of curves of I_{DS} as a function of V_{DS} for various values of V_{GS}. The curves illustrate performance of a typical inventive field effect transistor having the configuration of FIGURE 5.

FIGURE 7 is a greatly enlarged, top plan view of a four-terminal N-channel FET, yet another embodiment of the present invention.

FIGURE 8 is a graph of I_{DS} versus V_{DS} for a typical FET having the configuration illustrated in FIGURE 7.

One embodiment of the inventive N-channel enhancement mode field effect transistor is illustrated in FIGURE 1. As shown therein, a transistor 10 is fabricated on bulk semiconductor substrate 12, preferably having low acceptor concentration on the order of 10^{14} to 10^{15} impurity atoms per cubic centimeter. Disposed on upper surface 14 of semiconductor body 12 is a film 16 of electrically insulating material. Typically, film 16 is an oxide of the semiconductor of body 12, thus should body 12 comprise silicon, layer 16 may comprise SiO_2. Body 12 contains N-type source 18 and drain 20. Typically, source 18 and drain 20 may exhibit a donor impurity surface concentration on the order of 10^{20} atoms per cubic centimeter.

Electrical connection to source 18 is provided by means of electrode 22, while electrical connection to drain 20 is provided

by electrode 24. The region within semiconductor body 12 between source 18 and drain 20 comprises channel 26. The portion 16' of insulating layer 16 above channel 26 electrically insulates gate electrode 28 from channel 26.

In accordance with the present invention, P+ region 30 is provided completely surrounding source 18, isolating source 18 from channel 26.

Note that P+ region 30 extends a fraction of the length of channel 26, and the entire width of channel 26. The length of the channel is horizontal in the plane of the paper in Fig. 1 while the width is perpendicular to the plane of the paper. Typically, region 30 may have a surface concentration on the order of 5×10^{18} acceptor impurity atoms per cubic centimeter.

As discussed hereinabove, prior art enhancement mode FET's were characterized by current I_{DS} flow from source to drain even in the absence of an applied voltage at the gate. In the FET 10 (see FIGURE 1) P+ region 30 completely isolates source 18 from channel 26, hence no electron current will flow between source 18 and drain 20 when no voltage is applied to gate terminal 28, even though positive interfacial charge may be present at the interface between channel 26 and gate insulation 16'.

When a sufficient positive voltage is applied to gate 28 (see FIGURE 1) electron flow will begin between source 18 and drain 20. The threshold voltage for an embodiment of inventive FET 10 having a channel 26 width of 10 mils, a channel 26 length of 10 microns, and a gate insulation 16' thickness of 1,000 Å SiO_2 is illustrated by the curve designated $V_{DS(THRESHOLD)}$ in FIGURE 2. As may be seen therein, source to drain current I_{DS} begins to flow when the drain 20 to source 18 voltage V_{DS} (measured with gate 28 tied to drain 20) reaches a value on the order of 2.5 volts.

FIGURE 2 also illustrates the drain 20 to source 18 breakdown voltage $V_{(BR)DSS}$ for the embodiment of FET 10 just described. The curve marked $V_{(BR)DSS}$ was measured with gate 28 connected to source 20, thus placing FET 10 in the cut-off condition. Note that for the typical embodiment described, FET 10 exhibits a breakdown voltage of greater than 40 volts, considerably higher than for prior art FET's utilizing a highly doped channel.

The drain-source current I_{DS} as a function of drain-source voltage V_{DS} for various values of gate-source voltage V_{GS} is illustrated by a family of curves in FIGURE 3, as measured for typical FET 10 having a channel width of 10 mils, channel length of 10 microns, and gate insulation thickness of 1,000 Å. As shown in FIGURE 3, in the low current region, the drain current is somewhat linearly related to V_{DS}. As I_{DS} increases, the channel begins to deplete for a given value of V_{GS} and the slope of the I_{DS} curve decreases until saturation is reached, whereafter I_{DS} stays relatively constant until the drain-to-gate avalanche voltage is reached. Note that for increasing values of V_{GS} saturation is reached at a higher value of V_{DS}. Note also that a positive V_{GS} is required to initiate conduction of the inventive transistor 10, i.e., there is no current flow I_{DS} until threshold is reached. Operation is completely in the enhancement mode.

The difference ΔV_T in threshold value $V_{GS(THRESHOLD)}$ between transistor 10 fabricated in accordance with the present invention and a prior art transistor having similar channel length and width but not having P+ isolation region 30 is illustrated by the graph of FIGURE 4. Curve 32 shows the square root of I_{DS} plotted as a function of V_{GS} for a prior art transistor having no P+ isolation region 30, while curve 34 is plotted for a transistor 10 in accordance with the present invention and having substantially the same channel length and width as the transistor characterized by curve 32. As indicated by curve 32, with no voltage applied to the gate ($V_{GS} = 0$) considerable current flowed between source and drain of the prior art transistor, however, with $V_{GS} = 0$, no source to drain current flows in inventive transistor 10 (see curve 34). As indicated in FIGURE 4, the difference in threshold voltage ΔV_T is on the order of 5.3 volts.

Note that the transistor 10 is extremely attractive for digital applications, since when no voltage applied to the gate (i.e., $V_{GS} = 0$) essentially no I_{DS} flows; conversely, when an appropriate voltage V_{GS} is applied to gate 28, considerable current flows between source 18 and drain 20.

Referring once again to FIGURE 1, the field effect transistor 10 shown therein may be fabricated using the following exemplary process steps. Initially, body 12 of semiconductor material (e.g., silicon) having an acceptor concentration on the order of 10^{14} to 10^{15} impurity atoms per cubic centimeters is provided with dielectric coating 16. For example, layer 16 may be formed by the well known technique for thermally oxidizing surface 14 of silicon body 12 to form SiO_2. Appropriate source and drain diffusion openings then are provided in SiO_2 layer 16 using photolithographic techniques well known to those skilled in the art.

Next, a first diffusion of an acceptor type impurity such as boron is provided through the source opening only, an appropriate covering being provided over the drain diffusion opening. This acceptor diffusion produces P+ isolation region 30. Subse-

quently, N-type donor impurities are diffused simultaneously through both source and drain openings in insulating layer 16. Finally, electrodes 22, 24, and 28 are provided by vapour deposition of a metal such as aluminium through an appropriate mask.

Another embodiment of the field effect transistor is illustrated in FIGURE 5; this embodiment particularly lends itself to fabrication from a composite of silicon on sapphire.

Referring to FIGURE 5, a transistor 40 includes electrically insulating substrate 42, preferably of a single crystal material atop which a semiconductor may be grown epitaxially. Thus, substrate 42 may comprise single crystal sapphire, magnesium oxide, beryllium oxide, spinel or the like. Atop substrate 42 is disposed an island 44 of semiconductor material such as silicon, germanium, gallium arsenide, etc. In the embodiment shown, island 44 is of inherently P-type material into which has been diffused N-type source and drain regions 46 and 48. The region within semiconductor island 44 between source 46 and drain 48 comprises channel 50, however, note that source 46 is isolated from channel 50 by region 52 having a significantly higher P+ dopant concentration than that of the starting semiconductor material of island 44. Region 52 corresponds to the P+ isolation region 30 of the embodiment of the inventlon shown in FIGURE 1.

Channel 50 is covered by gate insulation film 54 such as silicon dioxide or the like. Gate electrode 56 is disposed atop passivation layer 54. Electrical connections to source 46 and drain 48 are made by means of electrodes 58*a* and 58*b*, respectively.

Performance characteristics for a typical field effect transistor 40 in accordance with the present invention and having the configuration illustrated in FIGURE 5 are shown in FIGURE 6. Analogous to FIGURE 3, FIGURE 6 contains a family of curves I_{DS} versus V_{DS} for various values of V_{GS}. Again, note that transistor 40 is characterized in having no source to drain current flow until an external gate voltage V_{GS} is applied.

Transistor 40 illustrated in FIGURE 5 may be fabricated utilizing generally the process described in British Patent Specification No. 1 069 506. However, analogous to the fabrication of the embodiment illustrated in FIGURE 1, P+ isolation region 52 is formed by an initial diffusion of P-type dopant through the source 46 mask opening prior to diffusion of source 46. Of course, the diffusion time to form isolation region 52 is longer than the diffusion time for source 46. This insures that the P+ dopant will progress further underneath passivation layer 54 than will the N-type donor material for source 46.

Embodiment 40 (see FIGURE 5) of the present invention has a total channel length defined by the distance between N-type source 46 and drain 48; heavily doped P+ isolation region 52 extends only a fraction of the total length of channel 50 (although region 52 extends the entire width of channel 50).

A four-terminal field effect transistor in accordance with the present invention, and fabricated in a semiconductor thin film atop an insulating substrate, is illustrated in FIGURE 7. Referring to FIGURE 7, transistor 80 includes substrate 82 of electrically insulating, single crystal material. Disposed stop substrate 82 is island 84 of P-type semiconductor material. Three regions are diffused into P-type island 84. First, N+ source 86 and drain 88 are formed; region 90 between source 86 and drain 88 then defines channel 90. Within channel 90 is defined by diffusion P+ isolation region 92 analogous to P+ isolation region 30 (see FIGURE 1) or P+ isolation region 56 (see FIGURE 5).

In the embodiment of FIGURE 7, P+ isolation region 92 extends to a lower portion 92′, direct electrical contact to which portion is made by metal contact 94. Gate electrode 96 is situated atop channel 90 and is insulated from regions 90 and 92 by passivation layer 97. In addition, metal electrodes 98 and 100 provide electrical contact respectively to source 86 and drain 88.

When the field effect transistor 80 (see FIGURE 7) is operated with electrical contact 94 serving as the control gate, much higher transconductance can be achieved than were insulated gate 96 used for control. Experimental structures of the type illustrated in FIGURE 7 have exhibited transconductance values an order of magnitude higher than conventional MOS transistors of the same channel length, channel width and gate insulation thickness.

Operating characteristics of a typical transistor 80 fabricated in accordance with the present invention are shown by the curves of I_{DS} versus V_{DS} in FIGURE 8. In each instance, a voltage of −15 volts was applied between insulated gate electrode 96 and source 98. The values of V_{BS} shown adjacent each of the curves of FIGURE 8 refer to the voltage applied between gate electrode 94 and source 98 (see FIGURE 7). Note that both positive and negative values of V_{BS} are shown in the family of curves, thus indicating that transistor 80 of FIGURE 7 will operate in the depletion as well as in the enhancement mode.

WHAT WE CLAIM IS:—

1. A field effect transistor including a channel, an N-type source and drain, and a P-type isolation region completely separ-

ating the source from the channel over the whole area of the source-channel junction so that, over the said area, current cannot flow between the source and channel other than through the isolation region.

2. A transistor as defined in claim 1, wherein the source comprises an N-type island diffused into a semiconductor body, and wherein the P-type isolation region completely surrounds the source.

3. A transistor as defined in claim 1, comprising a semiconductor island disposed on top of a single crystal, electrically insulating substrate, wherein the source, drain and P-type isolation region each extend through the entire thickness of the island.

4. A transistor as defined in claim 2, wherein the island is epitaxially grown on the substrate.

5. A transistor as defined in any of claims 1 to 4, wherein the isolation region has an acceptor impurity concentration substantially greater than the impurity concentration of the channel.

6. A transistor as defined in any of claims 1 to 5, wherein the channel is a P-type semiconductor.

7. A transistor as defined in any of claims 1 to 6, further comprising an electrode making electrical contact directly to the isolating region.

8. A transistor substantially as described with reference to Fig. 1 of the accompanying drawings.

9. A transistor substantially as described with reference to Fig. 5 of the accompanying drawings.

10. A transistor substantially as described with reference to Fig. 7 of the accompanying drawings.

11. A process for fabricating a transistor according to claim 1, comprising the steps of providing a diffusion mask on top of a semiconductor body, the mask having openings for source and drain diffusions, diffusing, through the source opening only, an acceptor type impurity to a first effective diffusion depth, and subsequently diffusing through the source and drain openings a donor type impurity to an effective diffusion depth less than the first effective diffusion depth.

12. A process as defined in claim 11, comprising the further steps of providing electrical contacts to the source and the drain, and providing an insulated gate electrode on top of the channel.

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1,224,335 COMPLETE SPECIFICATION
3 SHEETS

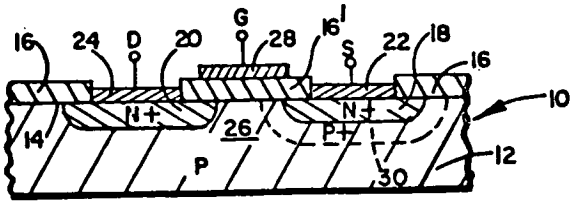


FIG. 1

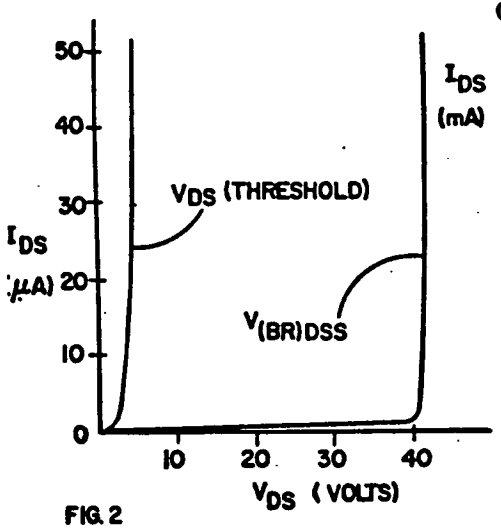


FIG. 2

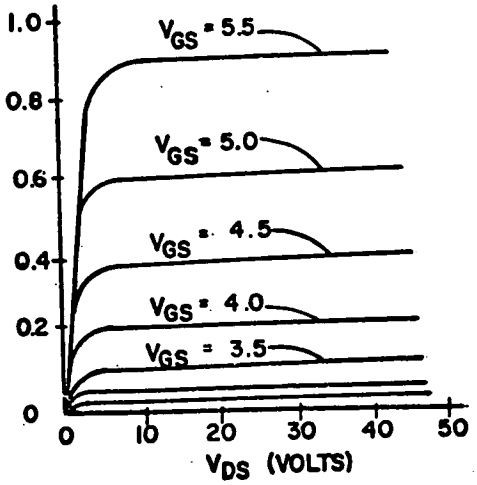


FIG. 3

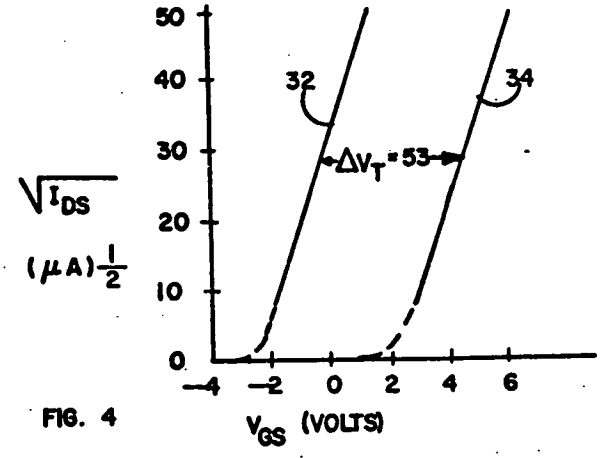


FIG. 4

FIG. 5

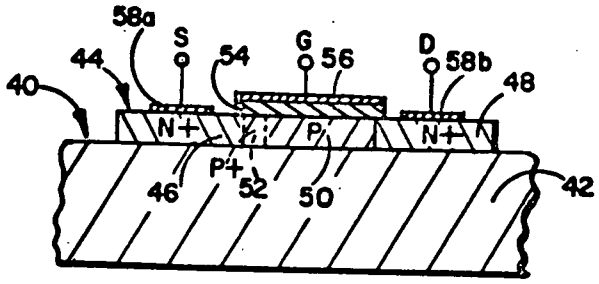
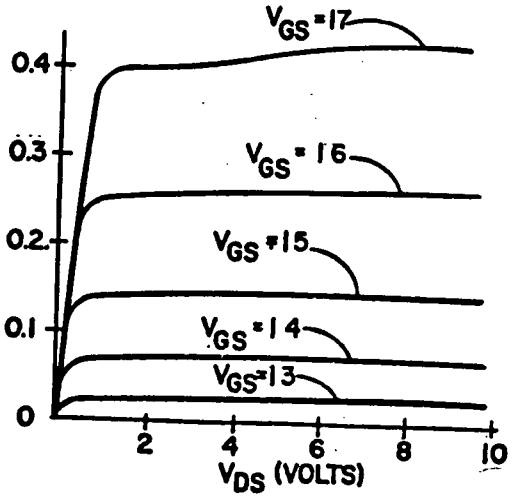

58a
S
44
54
G
56
D
58b
48
40
N+
P
N+
P+
46
52
50
42

FIG.6


I_{DS} (mA)
V_{GS}=17
V_{GS}=16
V_{GS}=15
V_{GS}=14
V_{GS}=13
0.4
0.3
0.2
0.1
0
2
4
6
8
10
V_{DS} (VOLTS)

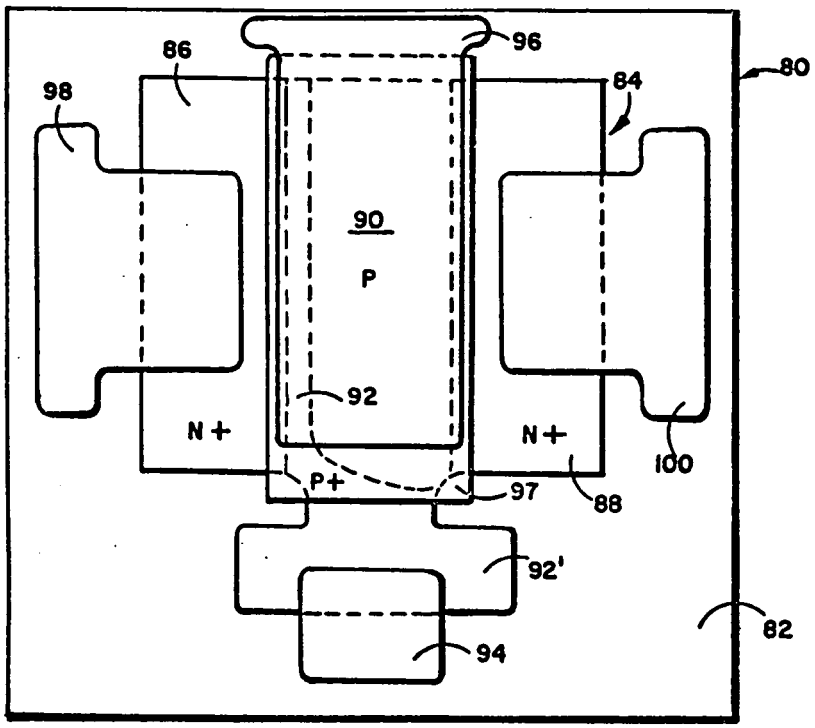

96
86
80
98
64
90
P
92
N+
N+
100
P+
97
88
92'
82
94

FIG. 7

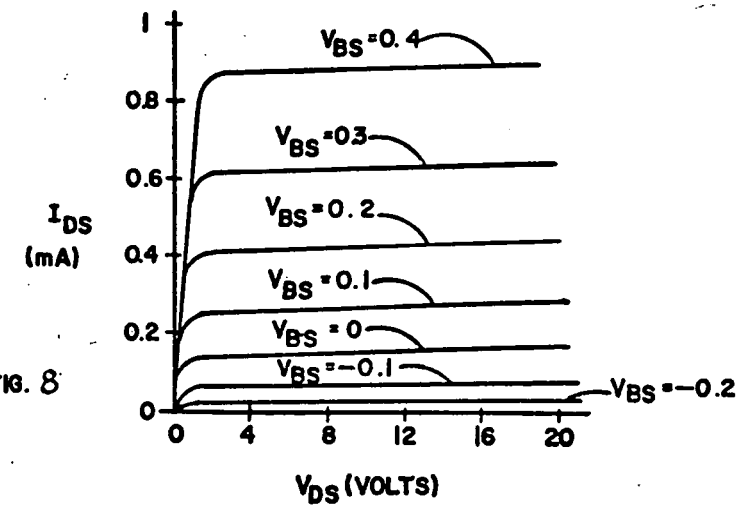

I
0.8
0.6
0.4
0.2
0
I_{DS} (mA)
V_{BS}=0.4
V_{BS}=0.3
V_{BS}=0.2
V_{BS}=0.1
V_{BS}=0
V_{BS}=−0.1
V_{BS}=−0.2
0
4
8
12
16
20
V_{DS} (VOLTS)

FIG. 8